REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
98-09-03

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, SOI, RADIATION- HARDENED, 32K x 8-BIT MASK PROGRAMMABLE ROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98644**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E478-98

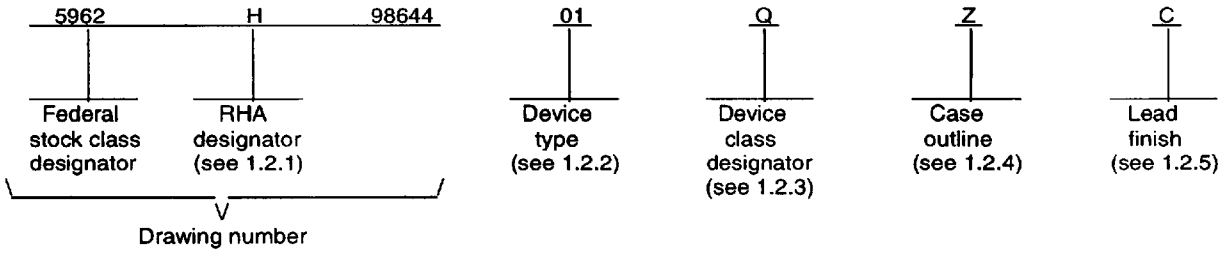
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0039663 0T0

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input buffer type	Access time
01	6656	32K X 8-bit radiation hardened mask PROM	CMOS	25 ns
02	6656	32K X 8-bit radiation hardened mask PROM	TTL	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	28	Flat package
Z	See figure 1	36	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage (V_{DD})	-0.5 V dc to +6.5 V dc
Voltage on any pin with respect to ground	-0.5 V dc to V_{DD} +0.5 V dc
DC output current (I_{OUT})	25 mA
Maximum power dissipation (P_D)	2.5 W
Lead temperature (soldering, 10 seconds maximum)	+270°C
Thermal resistance, junction-to-case (Θ_{JC}): Case Z	2.0°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Data retention	10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (V_{SS})	0.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Radiation features:	
Total dose irradiation,	≥ 1.0 MRads(Si)
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets	≥ 120 MEV-cm^2/mg
Neutron irradiation	1 x 10^{14} neutrons/cm^2 3/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100%

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Guaranteed, but not tested.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.4 AC test circuit and timing characteristics. The ac test circuit and timing characteristics shall be as specified on figure 4.

3.2.5 Read cycle waveforms. The read cycle waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6.

3.2.7 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific but shall guarantee data retention as specified in paragraph 1.3 over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the aquiring or preparing activity, along with test data.

3.3 AID requirements. All AID's written against this SMD shall be sent to DSCC-VAS. The following items shall be provided to the device manufacturer by the customer as part of an AID. These items form a part of the manufacturer's design database/database archive and shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 ROM mask definition. To generate a mask for a ROM code, an ASCII file shall be submitted. The format for the code shall be as follows:

a. Two fields, address followed by data in hexadecimal code, most significant bit to least significant bit (AH is most significant bit).

b. Addresses need not be in order.

c. Address and data fields must be separated by at least one space or a slash "/".

d. A semicolon ";" may terminate the line, but is not required.

e. No "end-of-file" characters are required.

f. Comments are preceded by the pound sign "#".

g. Comments may be on the same line **AFTER** address and data fields.

h. Unused locations do not need to be addressed, but **MUST** be specified as all zeroes or all ones. This can be done as a comment.

3.3.2 Fault coverage measurement of manufacturing logic tests.

3.3.3 Burn-in circuit.

3.3.4 Radiation exposure circuit.

3.3.5 Maximum device cross section for SEP.

3.3.6 Programmed devices. The truth table for final masked (programmed) devices shall be as specified in the altered item drawing.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID PIN shall be marked on the part and shall be in addition to the required marking of MIL-PRF-38535.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage	V_{OL1}	V_{DD} = 4.5 V, I_{OL} = 10 mA	1, 2, 3	All		0.4	V
		M,D,L,R,F,G,H	1 1/			2/	
	V_{OL2}	V_{DD} = 4.5 V, I_{OL} = 200µA	1, 2, 3	All		0.15	V
		M,D,L,R,F,G,H	1 1/			2/	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -200µA	1, 2, 3	All	V_{DD} - 0.1		V
		M,D,L,R,F,G,H	1 1/		2/		
	V_{OH2}	I_{OH} = -5.0mA	1, 2, 3	All	4.2		
		M,D,L,R,F,G,H	1 1/		2/		
Input low voltage CMOS inputs	V_{IL1}	V_{DD} = 4.5 V	1, 2, 3	01		0.3 x V_{DD}	V
		M,D,L,R,F,G,H	1 1/			2/	
Input low voltage TTL inputs	V_{IL2}	V_{DD} = 4.5 V	1, 2, 3	02		0.8	V
		M,D,L,R,F,G,H	1 1/			2/	
High-level input voltage CMOS inputs	V_{IH1}	V_{DD} = 5.5 V	1, 2, 3	01	0.7 x V_{DD}		V
		M,D,L,R,F,G,H	1 1/		2/		
High-level input voltage TTL inputs	V_{IH2}	V_{DD} = 5.5 V	1, 2, 3	02	2.2		V
		M,D,L,R,F,G,H	1 1/		2/		
Input leakage current	I_{ILK}	$0\ V \le V_{IN} \le 5.5\ V$	1, 2, 3	All	-5	5	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Three-state output leakage current	I_{OLK}	$0\ V \le V_{OUT} \le 5.5\ V$	1, 2, 3	All	-10	10	µA
		Output = high Z M,D,L,R,F,G,H	1 1/		2/	2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 2/ 3/	C_{IN}	$V_{IN} = V_{DD}$ or V_{SS}, f = 1 Mhz See 4.4.1c	4	All		9	pF
Output capacitance 2/ 3/	C_{OUT}	$V_{OUT} = V_{DD}$ or V_{SS}, f = 1 Mhz See 4.4.1c	4	All		14	pF
Functional tests		See 4.4.1d	7,8A,8B	All			
		M,D,L,R,F,G,H	1 1/				
Operating supply current (selected)	I_{DDOPR}	CE = $V_{IH} = V_{DD}$ 4/ f = 1MHz, I/O = 0, NCS = $V_{IL} = V_{SS}$	1, 2, 3	All		4.0	mA
		M,D,L,R,F,G,H	1 1/			2/	
Operating supply current (deselected)	I_{DDSBMF}	f = 1MHz, I/O = 0, $V_{IL} = V_{SS}$ 4/ NCS = CE = $V_{IH} = V_{DD}$	1, 2, 3	All		1.5	mA
		M,D,L,R,F,G,H	1 1/			2/	
Standby supply current	I_{DDSB1}	$V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, I/O = 0, inputs stable 5/	1, 2, 3	All		1.5	mA
		M,D,L,R,F,G,H	1 1/			2/	
Standby supply current (with chip disabled)	I_{DDSB2}	CE = V_{SS} or NCS = V_{DD}, I/O = 0 $V_{SS} \le V_{IL} \le V_{DD}$ 5/	1, 2, 3	All		1.5	mA
		M,D,L,R,F,G,H	1 1/			2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address read cycle time	t_{AVAVR}	See figure 4 and 5 6/	9, 10, 11	All	25		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address access time	t_{AVQV}		9, 10, 11	All		25	ns
		M,D,L,R,F,G,H	9 1/			2/	
Address change to output invalid time	t_{AXQX}		9, 10, 11	All	3		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip select access time	t_{SLQV}		9, 10, 11	All		35	ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip select output enable time	t_{SLQX}		9, 10, 11	All	5		ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip select output disable time	t_{SHQZ}		9, 10, 11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip enable access time 7/	t_{EHQV}		9, 10, 11	All		35	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip enable output enable time 7/	t_{EHQX}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip enable output disable time 7/	t_{ELQZ}		9, 10, 11	All		20	ns
		M,D,L,R,F,G,H	9 1/			2/	
Output enable access time	t_{GLQV}		9, 10, 11	All		9	ns
		M,D,L,R,F,G,H	9 1/			2/	
Output enable output enable time	t_{GLQX}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output enable output disable time	t_{GHQZ}		9, 10, 11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	ns

1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C$. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
3/ Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
4/ All inputs switching. DC average current.
5/ These parameters may not be tested, but shall be guaranteed to the values specified in table I.
6/ Test conditions assume input pulse levels of $V_{IL}/V_{IH} = V_{SS}/V_{DD}$ (CMOS), $V_{IL}/V_{IH} = V_{SS}/V_{DD}$ (TTL), input rise and fall times of ≤ 5.0 ns, input and output timing reference levels as shown in figure 4, capacitive output loading $C_L = 50$ pF.
7/ These tests are not applicable to devices supplied to package "Y".

Case Y

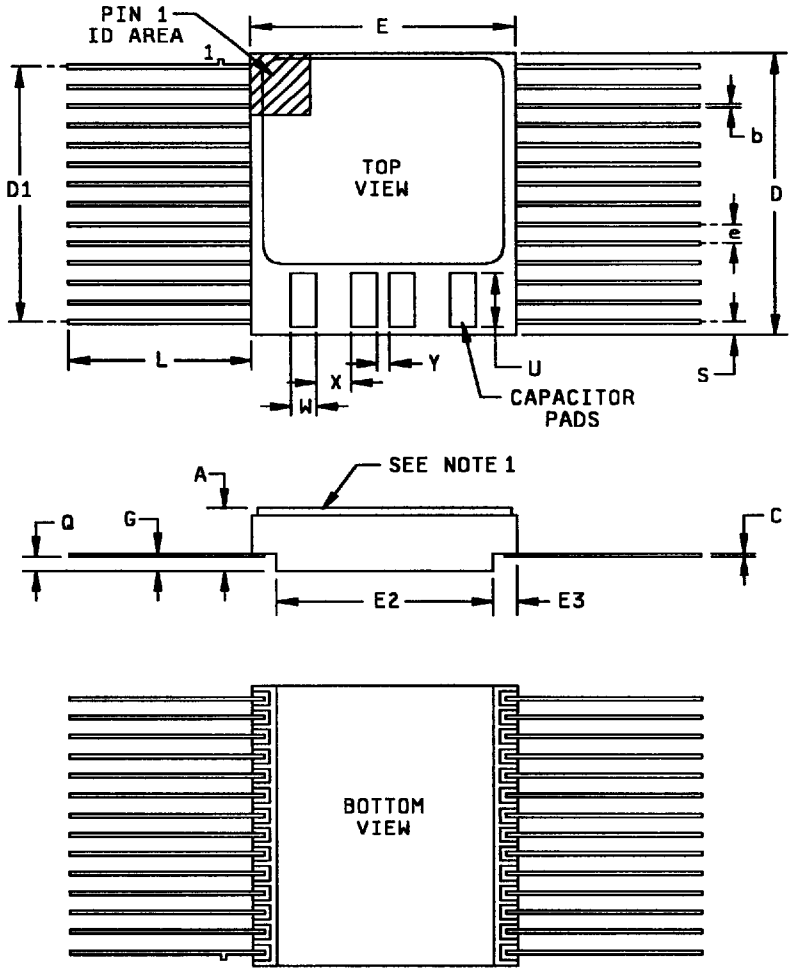


FIGURE 1. Case outlines - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE **A**		**5962-98644**
		REVISION LEVEL	SHEET **10**

DSCC FORM 2234
APR 97

9004708 0039672 003

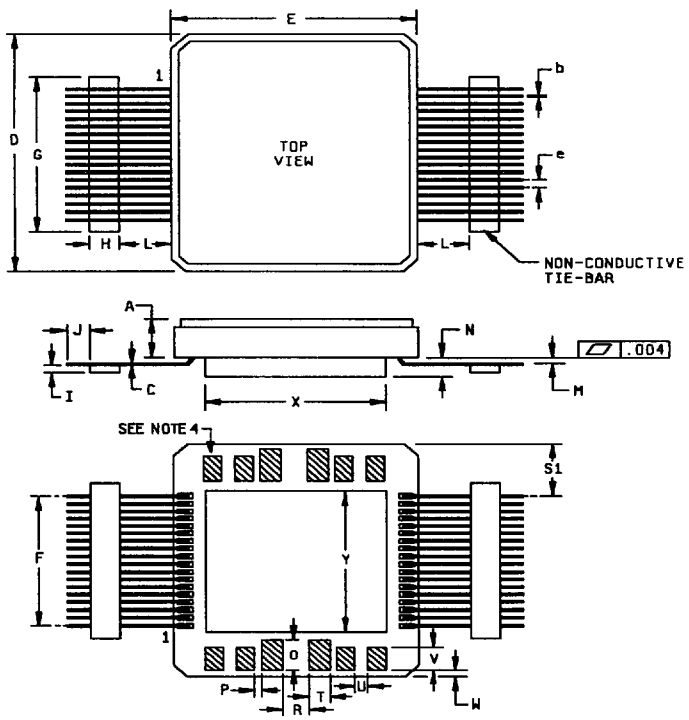
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.48	.015	.019
C	0.08	0.15	.003	.006
D	18.08	18.49	.712	.728
D1	16.38	16.64	.645	.655
E	12.52	12.88	.493	.507
E2	9.45	9.86	.372	.388
E3	1.52 REF		.060 BSC	
e	1.27 BSC		.050 BSC	

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
G	0.79	0.99	.031	.039
L	7.49	---	.295	---
Q	0.66	1.14	.026	.045
S	0.89	1.40	.035	.055
U	3.30 REF		.130 REF	
W	1.27 REF		.050 REF	
X	1.91 REF		.075 REF	
Y	0.25 REF		.010 REF	

NOTES: 1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P4.
3. Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outlines.

Case Z



Symbol	Inches 1/		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.085	.105	2.16	2.67	M	.005	.011	.13	.28
b	.006	.010	.15	.25	N	.040	.060	1.02	1.52
C	.005	.0075	.13	.19	O	.090 ref.		2.29	
D	.640	.660	16.26	16.76	P	.015 ref.		.38	
e	.023	.027	.58	.69	R	.075 ref.		1.91	
E	.623	.637	15.82	16.18	S1	.103	.123	2.62	3.12
F	.420	.430	10.67	10.92	T	.050 ref.		1.27	
G	.520	.530	13.21	13.46	U	.030 ref.		.76	
H	.130	.140	3.30	3.56	V	.080 ref.		2.03	
I	.025	.035	.64	.89	W	.005 ref.		.13	
J	.080 ref.		2.03		X	.450 ref.		11.43	
L	.270	.300	6.86	7.62	Y	.400 ref.		10.16	

Notes: 1/ Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2/ Parts delivered with leads unformed.
3/ Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface. Package lid is connected to V_{SS}.
4/ The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P12.

FIGURE 1. Case outline - continued.

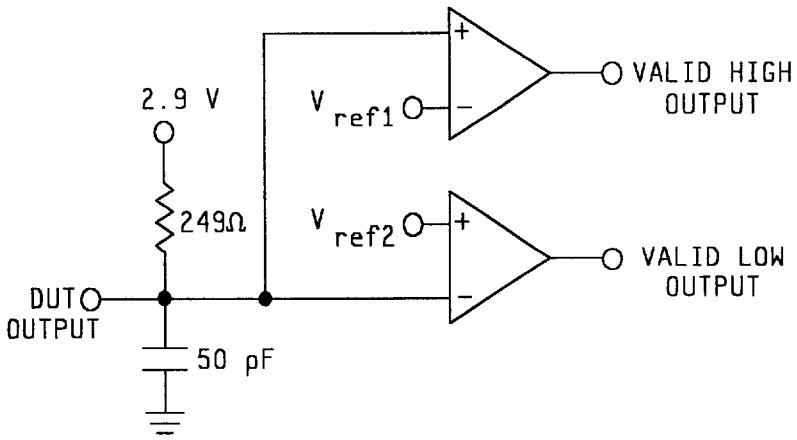
Device types	ALL	
Case outline	Y	Z
Terminal number	Terminal symbol	
1	A_{14}	V_{SS}
2	A_{12}	V_{DD}
3	A_7	A14
4	A_6	A12
5	A_5	A7
6	A_4	A6
7	A_3	A5
8	A_2	A4
9	A_1	A3
10	A_0	A2
11	DQ_0	A1
12	DQ_1	A0
13	DQ_2	DQ0
14	V_{SS}	DQ1
15	DQ_3	DQ2
16	DQ_4	NC
17	DQ_5	V_{DD}
18	DQ_6	V_{SS}
19	DQ_7	V_{SS}
20	NCS	V_{DD}
21	A_{10}	DQ3
22	NOE	DQ4
23	A_{11}	DQ5
24	A_9	DQ6
25	A_8	DQ7
26	A_{13}	NCS
27	NC	A10
28	V_{DD}	NOE
29	---	A11
30	---	A9
31	---	A8
32	---	A13
33	---	CE
34	---	NC
35	---	V_{DD}
36	---	V_{SS}
P1	---	---
P2	---	---
P3	---	---
P4	---	---
P5	---	---
P6	---	---
P7	---	---
P8	---	---
P9	---	---
P10	---	---
P11	---	---
P12	---	---

FIGURE 2. Terminal connections.

Mode	NCS	CE 1/	NOE 2/	Q
Read	Low	High	Low	Data-out
Deselected	High	X 3/	X	High-Z
Disabled	X	Low	XX 3/	High-Z

NOTES:
1/ CE is not applicable to devices supplied to package "Y".
2/ NOE = H: High Z output maintained for NCS = X, CE = X
3/ X: $V_I = V_{IH}$ or V_{IL}
4/ XX: $V_{SS} \leq V_I \leq V_{DD}$

FIGURE 3. Truth table.



	TTL I/O CONFIGURATION	CMOS I/O CONFIGURATION
INPUT LEVELS	V_{DD}, 0 V, $V_{DD}/2$	V_{DD}, 0 V, $V_{DD}/2$
OUTPUT SENSE LEVELS	1.5 V; V_{DD}-0.4 V, 0.4 V, HIGH Z; HIGH Z, 3.4 V, 2.4 V; HIGH Z = 2.9 V	$V_{DD}/2$; V_{DD}-0.4 V, 0.4 V, HIGH Z; HIGH Z, 3.4 V, 2.4 V; HIGH Z = 2.9 V

FIGURE 4. Output load circuit (or equivalent) and ac timing characteristics.

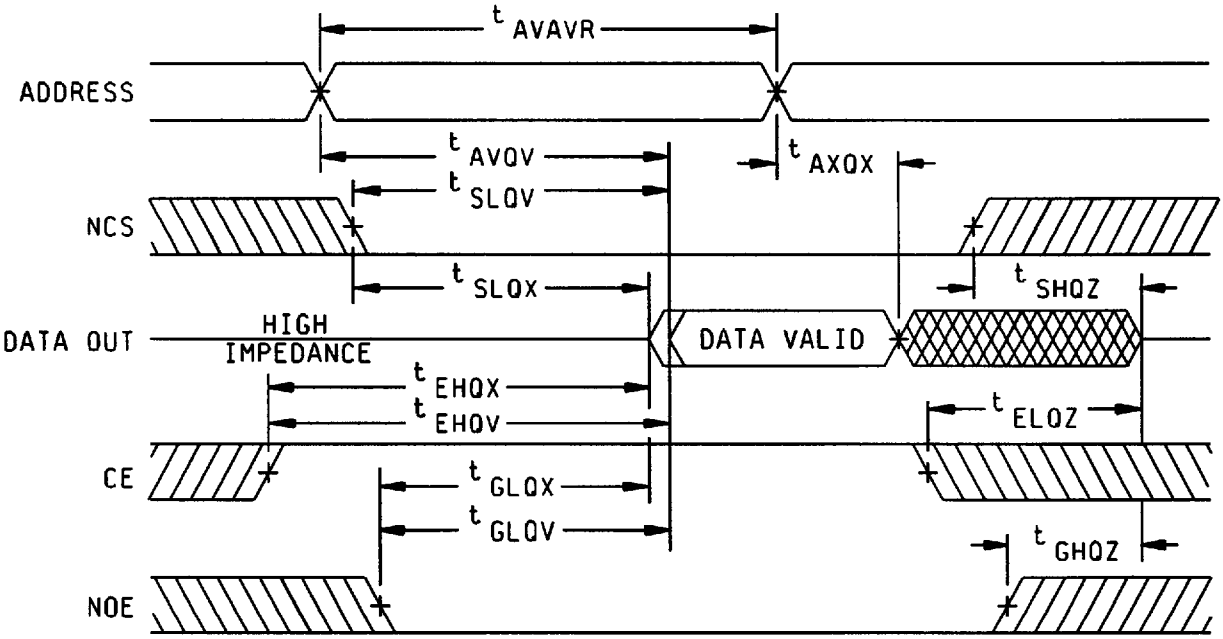
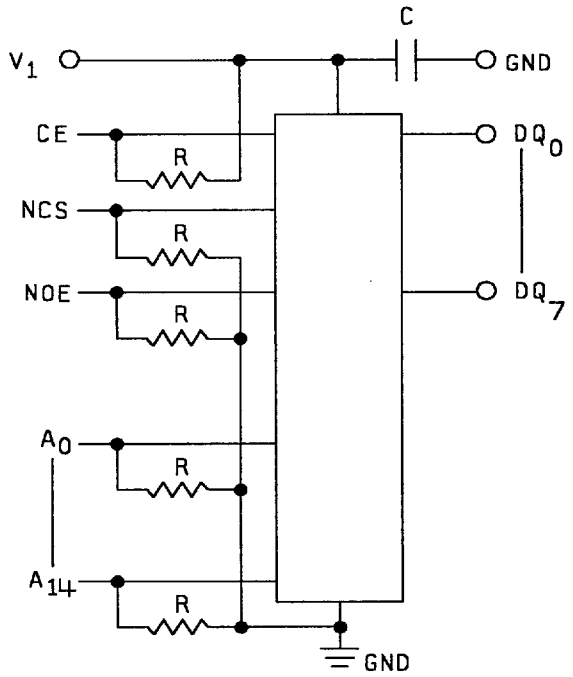


FIGURE 5. Read cycle waveform.



NOTES: 1. NCS, NOE, and A_0 through A_{14} = GND ; V_1 and CE = V_{CC}; DQ_0 through DQ_7 = floating; R = 10kΩ ± 10%; C = 0.1 µF ± 10%; V_{CC} = 5.0 V.
2. Power pins are connected to V_1.
3. The absolute voltage ratings of paragraph 1.3 shall not be exceeded.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging tests.
5. CE terminal is not applicable to devices supplied to package "Y".

FIGURE 6. Irradiation circuit.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Sample size is 5 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device as described in the AID. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein. The total dose level shall be greater than 1E6 rads(Si) at levels up to and including the level indicated, T_A = 25°C.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup immunity shall be guaranteed by design under recommended operating conditions.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

c. The transient dose rate upset level shall be greater than or equal to 5E10 rads(Si)/s with a pulse width less than or equal to 1.0 µs.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

Table IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table IA)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I method 1015	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10,11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10,11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IIA).
7/ See 4.4.1e.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{DDSB1}, I_{ILK}, I_{OLK}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

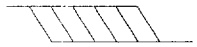
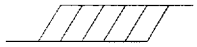
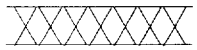
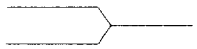
6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Symbols, definitions, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{DD} ..... Supply current.
I_I ..... Input current.
I_O ..... Output current.
T_C ..... Case temperature.
V_{DD} ..... Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-09-03

Approved sources of supply for SMD 5962-98644 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9864401QYC 5962H9864401QZC	34168	HX6656/NQHC HX6656/XQHC
5962H9864401VYC 5962H9864401VZC	34168	HX6656/NVHC HX6656/XVHC
5962H9864402QYC 5962H9864402QZC	34168	HX6656/NQHT HX6656/XQHT
5962H9864402VYC 5962H9864402VZC	34168	HX6656/NVHT HX6656/XVHT

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell, Solid State Electronics Center 12001 State Highway 55 Plymouth, MN 55441-4799

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.